a transmission line having a first end with a first characteristic impedance, a second end with a second characteristic impedance, and a quiescent voltage at ground voltage;

a first termination device connected to the first end of the transmission line and connected to ground to provide an impedance substantially matched to the first characteristic impedance of the transmission line;

a second termination device connected to the second end of the transmission line and connected to ground to provide an impedance substantially matched the second characteristic impedance of the transmission line; and

a first agent connected to the transmission line, the first agent comprising a die having a first core voltage, the die comprising a pMOSFET comprising a source at the first core voltage and a drain connected to the transmission line.

23. (New) The electronic system as set forth in claim 22, further comprising:

a second agent connected to the transmission line, the second agent comprising a die having a second core voltage, the die of the second agent comprising a pMOSFET comprising a source at the second core voltage and a drain connected to the transmission line.

24. (New) The electronic system as set forth in claim 23, wherein the first core voltage is not equal to the second core voltage.

25. (New) The electronic system as set forth in claim 24, wherein the first agent is connected at the first end of the transmission line, and wherein the first termination device is integrated on the die of the first agent.

26. (New) The electronic system as set forth in claim 25, wherein the second agent is connected to the transmission line at neither the first nor second end of the transmission line.

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27. (New) The electronic system as set forth in claim 23, wherein the first agent is connected at the first end of the transmission line, and wherein the first termination device is integrated on the die of the first agent.

28. (New) The electronic system as set forth in claim 27, wherein the second agent is connected to the transmission line at neither the first nor second end of the transmission line.

29. (New) The electronic system as set forth in claim 22, wherein the first agent is connected at the first end of the transmission line, and wherein the first termination device is integrated on the die of the first agent.

30. (New) The electronic system as set forth in claim 22, wherein the first agent is connected to the transmission line at neither the first nor second end.

31. (New) An electronic system comprising:

a ground having a ground voltage;

a transmission line having a termination device connected to ground to reduce signal reflections such that the transmission line has a quiescent voltage at ground voltage;

a die having a core voltage and comprising:

a pMOSFET driver to drive the transmission line, the pMOSFET driver having a source biased to the core voltage;

a nMOSFET driver coupled to the transmission line, the nMOSFET driver having a source at the ground voltage; and

a combinational logic circuit coupled to the nMOSFET driver.

32. (New) The electronic system as set forth in claim 31, wherein the combinational logic circuit is coupled to the nMOSFET driver so that the nMOSFET driver has a first ON resistance when the pMOSFET driver is ON and a second ON resistance when the pMOSFET driver is OFF, wherein the first and second ON resistances are not equal to each other.

33. (New) The electronic system as set forth in claim 31, the transmission line having a characteristic impedance, wherein the pMOSFET driver and nMOSFET in combination have an impedance substantially matched to the characteristic impedance of the transmission line if both the pMOSFET driver and nMOSFET driver are switched ON,

and wherein the nMOSFET has an impedance substantially matched to the characteristic impedance of the transmission line if the pMOSFET driver is switched OFF.

34. (New) An electronic system having a ground voltage, the electronic system comprising:

a transmission line having a characteristic impedance and a quiescent voltage at ground voltage; and

an integrated circuit die having a core voltage and comprising:

an input/output port connected to the transmission line;

a termination device to provide an impedance substantially matched to the characteristic impedance of the transmission line and having a first terminal connected to the input/output port and a second terminal at the ground voltage; and

a pMOSFET comprising a source at the core voltage and a drain connected to the input/output port.

35. (New) An electronic system comprising:

a ground having a ground voltage;

a transmission line having a first end, a second end, a characteristic impedance, and a quiescent voltage at ground voltage;

a first termination device connected to the first end of the transmission line and connected to ground to provide an impedance substantially matched to the characteristic impedance of the transmission line;

a second termination device connected to the second end of the transmission line and connected to ground to provide an impedance substantially matched to the characteristic impedance of the transmission line; and

a pMOSFET driver connected to the transmission line at neither the first nor second end to drive the transmission line to a voltage not at ground.

36. (New) The electronic system as set forth in claim 35, further comprising:

a nMOSFET driver connected to the transmission line to provide an impedance path to ground; and

a combinational logic circuit coupled to the nMOSFET driver so that the nMOSFET driver has a first ON resistance when the pMOSFET driver is ON and a second ON resistance when the pMOSFET driver is OFF, wherein the first and second ON resistances are not equal to each other.

37. (New) The electronic system as set forth in claim 35, further comprising

a nMOSFET driver connected to the transmission line, wherein the pMOSFET driver and the nMOSFET driver in combination have an impedance substantially matched to the characteristic impedance of the transmission line if both the pMOSFET driver and the nMOSFET driver are switched ON, wherein the nMOSFET driver has an impedance substantially matched to the characteristic impedance of the transmission line if the pMOSFET driver is switched OFF.

38. (New) An electronic system comprising:

a ground having a ground voltage;

a transmission line having a characteristic impedance and a quiescent voltage at ground voltage;

a pMOSFET driver connected to the transmission line;

a nMOSFET driver connected to the transmission line to provide an impedance path to ground; and

a combinational logic circuit coupled to the nMOSFET driver so that the nMOSFET driver has a first ON resistance when the pMOSFET driver is ON and a second ON resistance when the pMOSFET driver is OFF, wherein the first and second ON resistances are not equal to each other.

39. (New) An electronic system comprising:

a ground and a ground voltage;

a transmission line having a characteristic impedance and a quiescent voltage at ground voltage;

a pMOSFET driver connected to the transmission line; and

a nMOSFET driver connected to the transmission line to provide an impedance path to ground;

wherein the pMOSFET driver and the nMOSFET driver in combination have an impedance substantially matched to the characteristic impedance of the transmission line if both the pMOSFET driver and the nMOSFET driver are switched ON, and wherein the nMOSFET driver has an impedance substantially matched to the characteristic impedance of the transmission line if the pMOSFET driver is switched OFF.